Energy-efficient High-speed Links Using BER-optimal ADCs

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Abstract—We recently explored the concept of using BER-optimal ADCs for high-speed links. In this paper, we study the benefits of BER-optimal ADCs in terms of power savings and relaxation of component specifications in a 90 nm 1.2 V CMOS process. These analyses are based on component models for a flash ADC that capture bandwidth limitation of pre-amplifiers and metastability of latches. We show that in the presence of these ADC non-idealities, a 3-bit BER-optimal ADC can provide a 3 dB ADC shaping gain over a 4-bit conventional ADC. The one bit reduction offers power savings of 75% in the VGA and 50% in the ADC. Further, the 3 dB ADC shaping gain can be traded-off for a 50% reduction in transmit driver power, a 75% reduction of the pre-amplifier bandwidth, or a saving of one latch stage that leads to a 20% additional power reduction in the ADC.

I. INTRODUCTION

Analog-to-digital converter (ADC)-based receivers have emerged in multi-GS/s high-speed links, enabling the application of digital signal processing techniques for signal detection under more pronounced channel impairments [1], [2]. Figure 1(a) depicts a typical ADC-based back-plane link, where the ADC is conventionally treated as independent of the subsequent digital processor, and is designed to be a transparent conduit of the analog waveform $x(t)$. A key performance metric for the conventional ADC is thus the difference between its input and output, captured by the signal-to-noise-and-distortion-ratio (SNDR), which is strongly dependent on the number of ADC bits $B_X$.

For flash ADCs, a preferred architecture for high-speed links, the ADC area, power consumption, and input capacitance increase exponentially with $B_X$. Stringent specifications on ADC components is also imposed by the signal fidelity-based performance metrics, e.g., large pre-amplifier bandwidth and multiple stages of latches, all of which exacerbate the ADC power consumption, and make the design of low-power and high-speed ADCs a major challenge in ADC-based high-speed link design [3].

We recently proposed using BER-optimal ADCs for high-speed links [4], [5], where the quantization thresholds of a BER-optimal ADC are set to minimize the bit-error-rate (BER), the ultimate system-level metric of a high-speed link. The BER-optimal ADC is distinct from the prevailing digitally assisted ADCs [6], [7], as the former exploits a system-level view of the analog and mixed-signal components in a communication link, while the latter focusses only to improve the component-level and signal fidelity-based metrics. The BER-optimal ADC also differs from so called “analog-to-information” converters proposed for compressive sampling [8]: although both techniques can relax the specifications of analog and mixed-signal components in a sampling system, the latter only works with sparse analog signals but the communication signals discussed here are not necessarily sparse.

As shown in [4], the ADC shaping gain, defined as the reduction in required SNR to achieve the same BER as a conventional (uniform) ADC, offered by a 3-bit BER-optimal ADC over a 3-bit uniform ADC ranges from 2.5 dB for low ISI channels to more than 30 dB for high ISI channels. Moreover, a 3-bit BER-optimal ADC can even offer a 3 dB ADC shaping gain over a 4-bit uniform ADC. These results were obtained with the assumption that the ADC components are ideal, i.e., a sampler with infinite bandwidth, followed by a quantizer without metastability, as shown in Fig. 1(b).

In this paper, we study the benefits of a BER-optimal ADC in the presence of practical circuit-level non-idealities in a 90 nm, 1.2 V, CMOS process, and evaluate its impact on power savings and relaxation of ADC component specifications. We
first propose a system-level flash ADC model that captures major circuit non-idealities of the flash ADC, including the bandwidth limitation of pre-amplifiers and metastability in latches. Employing this model, we demonstrate that a) the benefits of the BER-optimal ADC are preserved in the presence of circuit non-idealities; b) the reduction of the number of ADC bits can be mapped not only to the power savings of the ADC itself, but also to that of the ADC driver; c) the ADC shaping gain can be traded-off for a savings in transmit driver power, or the relaxation of ADC components, e.g., the reduction of pre-amplifiers bandwidth, and the savings of latch stages with their clock drivers, each of which offers additional ADC power savings.

The proposed models including the VGA and the ADC components are described in Section II. In Section III, we compare the BER performance and power consumptions of the BER-optimal ADC and the conventional ADC in the context of a 6 Gb/s 1 m back-plane link, and propose strategies to relax the component specifications for further power savings. Conclusions are drawn in Section IV.

II. ANALOG FRONT END MODELING

A. VGA model

The variable gain amplifier (VGA) is the first stage of the analog front end, and acts as the ADC driver. Figure 2(a) shows a simplified VGA circuit, which can be modeled as a first order active low-pass filter shown in Fig. 2(b), with low frequency small signal gain \( A_V = g_m R_D \) and 3 dB bandwidth \( B = (2\pi R_D C_L)^{-1} \), where \( C_L \) is the output capacitance, and \( R_D \) is the load resistor. The power consumption of the VGA is

\[
P = V_{DD} I_{ss} = V_{DD} (2\pi C_L A_V B)^2 / (2k'W/L), \tag{1}
\]

where \( k' \) is a technology parameter, \( W/L \) is the width-to-length ratio of transistors \( M_{1,2} \). For a specific back-plane channel, \( A_V \) is fixed, and \( B \) is usually designed around 0.7/T with 1/T being the symbol rate; therefore, the power consumption of the VGA is proportional to the square of \( C_L \).

B. Flash ADC Architecture

Figure 3 shows the architecture of a typical \( B_X \)-bit flash ADC. The input signal is compared with \( N = 2^{B_X} - 1 \) quantization thresholds \( t = \{ t_k \}_{k=1}^N \) through \( N \) parallel comparators, each consisting of a pre-amplifier and multiple stages of latches. The latches sample the pre-amplifier outputs and generate a thermometer code, which is then encoded into binary format. With a flash architecture, reducing the ADC precision by 1 bit results in a 50% power savings in the ADC, and a 50% reduction of the VGA output capacitance, which reduces the VGA power by 75% according to (1).

C. Pre-amplifier Model

Figure 4 shows a widely employed differential pre-amplifier for high-speed ADCs, which can also be modeled as a first order active low-pass filter shown in Fig. 2(b). Preamplifier bandwidth requirement in conventional flash ADCs is imposed by mismatch and metastability tolerances, as well as admissible third order distortion [9]. For \( 4 \leq B_X \leq 6 \), this bandwidth to sampling frequency ratio is usually set to 2 to 3. The power consumption of the pre-amplifier is the same as in (1) except for a scale factor of 2 accounting for the double differential pairs. It can be seen that a) the pre-amplifier power consumption is a quadratic function of its gain and 3 dB bandwidth; b) the bandwidth can be traded-off with the gain without increasing the pre-amplifier power consumption.

D. Cascaded Latch Stages Model

As shown in Fig. 3, multiple stages of latches are usually employed in high-speed flash ADCs to mitigate the impact of metastability of latches. The cascaded latch stages can be composed of several stages of amplifying latches, followed by a stage of full-swing storage latches that generate valid logic values for the following binary encoder.

The system-level behavior of the multiple stages of latches within each comparator can be described as

\[
V_{out}[n] = \begin{cases} 
\text{sgn} \left( V_{in}[n-D] \right) & \text{if} \ |V_{in}[n-D]| > \gamma \\
V_{out}[n-1] & \text{if} \ |V_{in}[n-D]| \leq \gamma 
\end{cases}, \tag{2}
\]
where \( V_{in} \) is the input voltage of the first stage of latch, \( V_{out} \) is the output voltage of the storage latch, \( D \) is the latency induced by the latch stages, and the threshold \( \gamma \) is determined by the transient behavior of each latch stage and the clock frequency, and can be obtained from circuit simulations. It is seen from (2) that if \( |V_{in}[n-D]| \) is smaller than \( \gamma \), \( V_{out}[n] \) will maintain its previous logic value even if \( V_{in}[n-D] \) has a different polarity, resulting in a metastability error.

E. ADC component power consumption

To verify the benefits of the BER-optimal ADC, we have designed a 4-bit 6 GS/s ADC based on the structure in Fig. 3, in a 90 nm, 1.2 V, CMOS LP process. Each comparator consists of one pre-amplifier, with the 3 dB bandwidth set to 2.2/T to meet the conventional design specification, followed by one stage of current mode latch and three stages of CMOS latches including the storage latch. Schematic simulations indicate that the power consumption of pre-amplifiers is 9.9 mW. The four stages of latches and their clock drivers consume 34.5 mW and 39.6 mW respectively, and each latch stage has similar power consumption. The encoder consumes 6 mW. Therefore, the total ADC power consumption is 90 mW, where the power consumption of the pre-amplifiers accounts for 11\%, and that of each latch stage and its clock driver accounts for about 9.6\% and 11\% respectively.

III. BER PERFORMANCE AND POWER SAVINGS

A. Simulation Setup

The simulations are based on a link shown in Fig. 1(a), with data rate of 6 GS/s over a 1 m back-plane channel [10]. The component models of the ADC are described in Section II. The sampled pre-amplifier output \( x_c[n] \) can be expressed as

\[
x_c[n] = \sum_{i=0}^{M-1} h[i] b[n-i] + v[n],
\]

where \( \{b[n]\}_{n=0}^{\infty} \) is a 2-PAM transmitted sequence taking values from \( \{\pm 1\} \), \( h[i] \) is the baud sampled composite impulse response including the pulse-shaping filter, back-plane channel, VGA, and the pre-amplifier, and \( v[n] \) is modeled as an additive white Gaussian noise source. The variance of \( v[n] \) is given by

\[
\sigma_v^2 = \int_{-\infty}^{\infty} \frac{N_0}{2} |H_{ch}(f)|^2 df,
\]

where \( N_0/2 \) is the power spectral density of \( n(t) \), and \( H_{ch}(f) \) is the composite transfer function of the VGA and the pre-amplifier. The 3 dB bandwidth of VGA is set to 0.7/T, and the SNR at the VGA output is given by

\[
SNR_{VGA} = \frac{\sum_{i=0}^{M-1} |h_{ch,VGA}[i]|^2}{\int_{-\infty}^{\infty} \frac{N_0}{2} |H_{VGA}(f)|^2 df},
\]

where \( H_{VGA}(f) \) is the transfer function of the VGA, and \( h_{ch,VGA}[i] \) is the baud sampled composite impulse response including the pulse-shaping filter, back-plane channel, and the VGA. A linear MMSE equalizer with \( L = 3 \) taps is employed, where the coefficient vector \( w \) is obtained according to \( \{h[i]\}_{i=0}^{M-1} \) and \( \sigma_v^2 \) with a 4-bit uniform ADC.

The BER can be computed by averaging over all possible ADC output vectors \( x = [x[n], \cdots, x[n-L+1]]^T \) such that \( b[n] \) is different from \( \hat{b}[n] = \sgn \left( w^T x \right) \), i.e.,

\[
BER = \sum_x \left( \prod_{j=0}^{L-1} \Pr \{x[n-j] = r_k\} \left( 1 - \frac{b[n]\hat{b}[n]}{2} \right) \right)
\]

and \( \Pr \{x[n-j] = r_k\} \) is given by

\[
Q \left( \frac{t_k - x_{c,0}[n-j]}{\sigma_v} \right) - Q \left( \frac{t_k - x_{c,0}[n-j]}{\sigma_v} \right),
\]

where \( x_{c,0} = \sum_{i=0}^{M-1} h[i] b[n-i] \) is the noiseless composite channel output, \( Q(\cdot) \) is the Gaussian Q function, \( r = \{r_k\}_{k=1}^{N+1} \) and \( t = \{t_k\}_{k=1}^{N} \) are the quantization levels and quantization thresholds of the ADC. The optimal \( r \) and \( t \) are obtained via gradient search, with \( \{h[i]\}_{i=0}^{M-1}, \sigma_v^2 \) and \( w \) as parameters, and BER as the cost function [4].

B. Impact of Pre-amplifier Bandwidth

Pre-amplifiers are among the most power hungry ADC components. The power dissipated by the single stage pre-amplifiers accounts for about 11\% of the total ADC power in our design as mentioned in Section II, and this percentage is even higher for ADCs with multiple stages of pre-amplifiers, e.g., about 30\% as reported in [11].

Figure 5 illustrates BER vs. SNR at the VGA output for a 3-bit BER optimal ADC with different pre-amplifier bandwidths, and a 4-bit conventional ADC with pre-amplifier bandwidth of 2.2/T. It is shown that even taking the finite bandwidth of the pre-amplifier into account, the 3-bit BER optimal ADC can achieve an ADC shaping gain of 4.6 dB over a 3-bit uniform ADC, and of 3 dB over a 4-bit uniform ADC, when all ADCs are assigned with the pre-amplifier bandwidth of 2.2/T. Furthermore, the pre-amplifier bandwidth of the 3-bit BER-optimal ADC can be reduced to 0.55/T, to achieve a BER still lower than that of the 4-bit conventional ADC with 2.2/T pre-amplifier bandwidth. This indicates about 94\% power savings in the pre-amplifiers, hence about 10\% additional power savings for the 3-bit BER-optimal ADC over the 4-bit uniform ADC according to our design, in addition to the 50\% power saving due to the 1-bit reduction.
C. Impact of Latch Metastability

As mentioned in Section II, metastability errors may occur in the comparators. Schematic simulations of our ADC show that $\gamma = 2.7\text{mV}$ in (2) when we have four stages of latches including the storage latch, and $\gamma$ becomes $12\text{mV}$ when we save the first stage of the current mode latch. Based on these threshold values, it is shown in Fig. 6 that with both pre-amplifier bandwidth limitation and metastability errors, the 3-bit BER optimal ADC preserves the 4.6 dB and 3 dB shaping gains over the 3-bit and 4-bit uniform ADCs, when all ADCs are assigned with the pre-amplifier bandwidth of $2.2/T$ and pre-amplifier gain of 2, and when four stages of latches are employed. In addition, the pre-amplifier bandwidth can further be reduced by 75% without changing the gain, for the 3-bit BER-optimal ADC to achieve lower BER than the 4-bit uniform ADC at a BER $< 10^{-12}$.

On the other hand, if the power consumption of the pre-amplifier is kept fixed, the gain of the pre-amplifier can be increased by reducing the pre-amplifier bandwidth under a fixed gain-bandwidth product, which improves the tolerance of the comparators against latch metastability. By doing so, one or more stages of latches can be removed without worsening the BER, thus offering additional power savings. For example, by relaxing the pre-amplifier bandwidth of the BER optimal ADC from $2.2/T$ to $0.55/T$, the pre-amplifier gain can be increased by fourfold. As illustrated in Fig. 6, this enables the 3-bit BER optimal ADC to not require the first stage of current mode latch, while still achieving a BER lower than that of a 4-bit conventional ADC with pre-amplifier bandwidth of $2.2/T$ and pre-amplifier gain of 2 at a BER $< 10^{-12}$. The resulting additional power savings is about 20% of the total ADC power, specifically, about 10% power savings due to the saved latch stage, plus another 10% corresponding to its clock driver power consumption.

D. Summary of Power Savings

We summarize the power savings of high-speed link components offered by the 3-bit BER-optimal ADC as compared to the 4-bit uniform ADC, according to our design. The one bit reduction of the ADC offers a 50% power savings in the ADC and a 75% power savings in the VGA, due to the flash architecture as analyzed in Section II. In addition, the ADC shaping gain provided by the BER-optimal ADC can be traded-off for additional power savings. First, the 3 dB shaping gain of the 3-bit BER-optimal ADC over the 4-bit uniform ADC can be directly mapped to a 50% power reduction in the transmit driver, without altering the ADC components. Alternatively, if the transmit power is unchanged, the shaping gain can be exploited for relaxing the specifications of the ADC components. For example, the pre-amplifier bandwidth can be reduced by 75% with a fixed gain for the 3-bit BER-optimal ADC to maintain the same BER as the 4-bit uniform ADC, offering a 10% additional ADC power savings. Yet another trade-off is to increase the pre-amplifier gain and reduce its bandwidth at a fixed pre-amplifier power consumption. In this case, the 3-bit BER-optimal ADC needs one less latch stage and their clock drivers to achieve the same BER as the 4-bit conventional ADC, offering a 20% additional power savings.

IV. Conclusion

This paper shows that the promise of the BER-optimal ADC is maintained even in the presence of ADC non-idealities such as finite pre-amplifier bandwidth and metastability in latches. We have also demonstrated that the BER-optimal ADC can reduce power consumption by relaxing the specifications of the ADC components.

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REFERENCES


